

**AMENDMENTS TO THE SPECIFICATION**

Please replace Paragraphs [0002] and [0003] with the following amended paragraphs:

[0002] This application is related to U.S. Patent Application Serial No. \_\_\_\_\_, filed \_\_\_\_\_ entitled No. 10/635,083, filed August 6, 2003, entitled GENERAL PURPOSE PERFORMANCE COUNTER; ~~(Docket No. 200208999-2)~~; U.S. Patent Application Serial No. \_\_\_\_\_, filed \_\_\_\_\_ entitled No. 10/635,371, filed August 6, 2003, entitled COVERAGE CIRCUIT FOR PERFORMANCE COUNTER; ~~(Docket No. 200208996-1)~~; U.S. Patent Application Serial No. \_\_\_\_\_, filed \_\_\_\_\_ entitled No. 10/635,372, filed August 6, 2003, entitled COVERAGE DECODER CIRCUIT FOR PERFORMANCE COUNTER; ~~(Docket No. 200208997-1)~~; U.S. Patent Application Serial No. \_\_\_\_\_, filed \_\_\_\_\_ entitled No. 10/635,103, filed August 6, 2003, entitled DATA SELECTION CIRCUIT FOR PERFORMANCE COUNTER; ~~(Docket No. 200209000-1)~~; U.S. Patent Application Serial No. \_\_\_\_\_, filed \_\_\_\_\_ entitled No. 10/635,079,

filed August 6, 2003, entitled ZEROING CIRCUIT FOR PERFORMANCE COUNTER; ~~(Docket No. 200209001-1);~~ and U.S. Patent Application Serial No. \_\_\_\_\_, filed \_\_\_\_\_ entitled No. 10/635,373, filed August 6, 2003, entitled MATCH CIRCUIT FOR PERFORMANCE COUNTER; ~~(Docket No. 200209002-1);~~ all of which are hereby incorporated by reference in their entirety.

Please replace Paragraph **[0024]** with the following amended paragraph:

**[0024]** Additional details regarding operation of the match/threshold circuit 202 are provided in U.S. Patent Application Serial No. \_\_\_\_\_, filed \_\_\_\_\_ entitled No. 10/635,373, filed August 6, 2003, entitled MATCH CIRCUIT FOR PERFORMANCE COUNTER. ~~(Docket No. 200209002-1).~~

Please replace Paragraph **[0026]** with the following amended paragraph:

**[0026]** Additional details regarding the operation of the sm\_sel circuit 204 and the szero circuit 206 are provided in U.S. Patent Application Serial No. \_\_\_\_\_, filed \_\_\_\_\_ ~~entitled No. 10/635,103, filed August 6, 2003, entitled DATA SELECTION CIRCUIT FOR PERFORMANCE COUNTER (Docket No. 200209000-1)~~ and U.S. Patent Application Serial No. \_\_\_\_\_, filed \_\_\_\_\_ ~~entitled No. 10/635,079, filed August 6, 2003, entitled ZEROING CIRCUIT FOR PERFORMANCE COUNTER. (Docket No. 200209001-1).~~

Please replace Paragraph **[0046]** with the following amended paragraph:

**[0046]** FIG. 6D depicts ~~[[an]]~~ another embodiment of ~~[[the]]~~ a portion of accumulation circuit ~~[[516]]~~ 510 illustrated in FIG. 5. In the illustrated embodiment of a subtract accumulation circuit 630, the same population count circuit implementation may

be used for both increments and decrements. A first population count circuit 632 receives the  $N$ -bit wide masked debug data signal from the inc\_mask circuit 506. Responsive thereto, the first population count circuit is operable to output a population value,  $P_1$ , which is based on the number of active inputs. This value is subsequently padded with the necessary number of zeros to provide a  $D$ -bit sum value,  $S_1$  where  $D$  can be 8, 16, etc. Similarly, a second population count circuit 634 receives the  $N$ -bit wide masked debug data signal from the dec\_mask circuit 508. Responsive thereto, the second population count circuit 634 is operable to output a population value,  $P_2$ , which is also padded with the necessary number of zeros to provide another  $D$ -bit sum value,  $S_2$ . The two  $D$ -bit sum values are subtracted from one another to provide a  $D$ -bit output value,  $S_3$ , which may be forwarded to the counter circuit of FIG. 5 for further processing.